UNITED STATES PATENT APPLICATION

FOR

HIGH SPEED DIGITAL PATH FOR SUCCESSIVE APPROXIMATION

ANALOG-TO-DIGITAL CONVERTERS

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BACKGROUND OF THE INVENTION

1.   Field of the Invention

5   The present invention relates to the field of successive

approximation analog-to-digital converters.

2.   Prior Art

A traditional successive approximation (SAR) analog-to-

digital converter (ADC) is schematically shown in Figure 1.

10   The specific converter shown uses a differential switched

capacitor DAC coupled to a comparator having an output

coupled to a successive approximation register controlling

non-overlapping switch drivers coupled to the switched

capacitor DAC. An analog input sample-and-hold is provided,

15   which may be the switched capacitor DAC itself, with the

overall SAR ADC being controlled by some form of controller

such as the state machine shown.

In a switched capacitor DAC, the capacitor values may be

in a binary sequence (radix = 2) with one terminal of all

20   capacitors connected to the DAC output. (Reduced radix and

mixed radix DACs are also known, to which the present

invention is equally applicable.) In a differential switched

capacitor DAC as shown, two single-ended DACs operate in

opposite polarity so that the outputs of the two DACs may be
compared by the comparator, rather than a single output
compared to ground as in a single-ended DAC. In operation,
the DAC output is switched to ground and the capacitors are

5   all simultaneously connected to and charged to the analog
input voltage in the analog input sample-and-hold circuit.
Then the grounding is removed and each capacitor is coupled
to a reference voltage, one at a time, starting from the most
significant bit (the largest capacitor). Typically the

10   capacitance representing the least significant bit is
replicated so that the capacitance of the most significant
bit is equal to the sum of all of the rest of the
capacitances. Thus when the switch drivers connect the
capacitance associated with the most significant bit to the

15   reference voltage, the comparator will reverse state if the
analog input voltage was less than half the reference
voltage, but will not reverse state if it is more than half
of the reference voltage V_{REF}. If the comparator does reverse
state, than the non-overlapping switch driver associated with

20   the most significant bit is reset (the capacitor reconnected
to the analog input signal), otherwise it is left set.
Either way, the comparator output will remain, or return,
respectively, to its original state. Then the next
overlapping switch driver is set, and left set if the output

25   of the converter does not change, or reset if the output of

the comparator does change, again after which the comparator will remain or return to its original state again. The sequence is repeated until the least significant bit is tested, after which the latches in the successive

5   approximation register controlling the non-overlapping switch drivers will contain the digital value of the analog input signal held in the analog input sample-and-hold. A more complete description of the operation of a switched capacitor DAC analog-to-digital converters may be found in "Bipolar and

10   MOS Analog Integrated Circuit Design" by Alan B. Grebene, a Wiley-Interscience Publication, 1984, starting on page 853.

       In such analog-to-digital converters, non-overlapping switch drivers are required to control the switches in the switched capacitor DAC for proper operation of the algorithm.

15   The speed of a successive approximation ADC is normally limited by the sum of the delays through the comparator, the successive approximation register, the non-overlapping drivers and switched capacitor DAC. Such delays can be substantial given the fact that the sequence must be repeated

20   in a non-overlapping fashion for each successive bit in each multiple bit conversion. Additional delays are introduced when level shifters are needed, as when the digital and analog portions of the circuit are driven from separate supply voltages. In that regard, level-shifting is often

25   used because high analog supply voltages are desirable for

performance reasons, but small-geometry digital CMOS gates often can't tolerate those larger voltages. Thus, it's often necessary to use larger geometry devices in the analog supply section and add level-shifting at some point between analog

5   and digital sections. Without level-shifting, a high input from the low-voltage section will not be high enough to completely turn off the PMOS devices, allowing static supply current to flow, potentially giving incorrect CMOS logic levels.

10   Figure 2 provides an example of a prior art implementation of a successive approximation register 20 and non-overlapping switch drivers 22 as separate functions. Each latch must set before the respective switch driver is initiated, and if the comparator output (Figure 1) changes

15   state, must reset before the switch drivers are themselves reset.

Figure 3 provides an example of a prior art implementation of a supply voltage level shift and non-overlapping switch driver as separate functions. The supply

20   voltage level shift is provided by flip-flop circuit 24 powered by typically a higher voltage supply and controlled by lower voltage inputs INPUT and $\overline{\text{INPUT}}$, which may be the Q and $\overline{\text{Q}}$ outputs of successive approximation latches as shown in Figure 2. The high voltage referenced output of the flip-

flop circuit is coupled to the non-overlapping switch drivers 26, also powered from the higher voltage supply.

The feedback connections in the level-shifter of Figure 3 perform the level-shift as follows. When NMOS transistor
5   Q2 is turned off and NMOS transistor Q1 is turned on, the gate of feedback PMOS transistor Q6 is pulled low, causing the gate of the PMOS transistor Q5 to be pulled all the way to the high supply voltage, completely turning off PMOS transistor Q5. Of course, when NMOS transistor Q1 is turned
10   off and NMOS transistor Q2 is turned on, the opposite sequence happens. The transistors must be sized so that the NMOS devices are strong enough to pull the output low initially until the feedback comes back and fully turns off the PMOS transistors Q5 or Q6.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram of a traditional successive approximation (SAR) analog-to-digital converter (ADC).

5   Figure 2 provides an example of a prior art implementation of successive approximation registers and non-overlapping switch drivers as separate functions.

Figure 3 provides an example of a prior art implementation of a supply voltage level shift and non-overlapping switch drivers as separate functions.

10   overlapping switch drivers as separate functions.

Figure 4 illustrates an embodiment of the present invention using combined set-reset latches and non-overlapping switch drivers.

Figure 5 illustrates a NOR gate based combined set-reset

15   latches and non-overlapping switch drivers.

Figures 6a through 6f are examples of some combined set-reset latches and switch drivers that may be used in the present invention.

Figure 7 illustrates a NOR gate based combined set-reset

20   latch and switch drivers duplicating the function of the NOR gate based combined set-reset latches and switch drivers of Figure 5 and further incorporating a level shift capability.

Figure 8 shows a generalized prior art level shifter and non-overlapping switch driver similar to that of Figure 3.

Figure 9 showing a generalized present invention circuit equivalent to that of Figure 8 and similar to that of Figure

5 7.

Figure 10 shows a generalized prior art latch and non-overlapping switch driver.

Figure 11 showing a generalized present invention latch and non-overlapping switch driver.

10 Figure 12 shows a prior art latch, level shifter and non-overlapping switch driver.

Figure 13 shows a generalized latch, level shifter and non-overlapping switch driver in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In a binary coded switched capacitor DAC, the capacitor values are in a binary sequence. However the present invention is also applicable to reduced radix and mixed radix

5   DACs. Accordingly, in the description to follow, the reference to a bit, unless the context indicates otherwise, refers to an internal bit of the ADC, which may or may not have a binary weighting, as is well known in the art.

Now referring to Figure 4, an exemplary embodiment of

10   the present invention also using a differential switched capacitor DAC may be seen (though the present invention is also applicable to ordinary or non-differential DACs). In accordance with this embodiment, the successive approximation registers and non-overlapping switch drivers of the prior art

15   (see Figure 1) are combined into set-reset latches and switch drivers, reducing the time of response on each successive approximation, thereby increasing the speed of operation of the ADC. Thus the output of the comparator is directly coupled to the SAR and NOL switch drivers (combined

20   successive approximation registers and non-overlapping switch drivers) and may be directly controlled by the state machine or other controller to control the switched capacitor DAC.

One embodiment of combined SAR and NOL switch drivers may be seen in Figure 5. A typical combined register bit and

associated switch driver is shown within dashed line 28.
This circuit, of course, is replicated for each bit of the
ADC as may be seen in Figure 4. The switch drivers are non-
overlapping in the positive logic sense that an OUTP(n) and

5   corresponding OUTM(n) are never both high, and in the
negative logic sense that an $\overline{\text{OUTP(n)}}$ and corresponding
$\overline{\text{OUTM(n)}}$ are never both low.

At the beginning of a conversion sequence, all the
BITSET signals from the state machine are low. A

10   GLOBAL_RESET pulse drives the output of NOR gate NOR1 low,
and thus the output of inverter I1 high, which provides the
output signal $\overline{\text{OUTP(N)}}$ to the switched capacitor array. The
high output of inverter I1 also drives the output of inverter
I2 low, providing the output signal OUTP(N). Thus both

15   inputs to NOR gate NOR2 are low, providing a high input to
inverter I3, which provides a low output for the signal
$\overline{\text{OUTM(N)}}$, with inverter I4 providing a high output for the
output signal OUTM(N) and providing a second high input to
NOR gate NOR1, thereby holding the latch and switch drivers

20   for bit N in the reset state after the GLOBAL_RESET signal
goes low. All other switch drivers are simultaneously reset
the same way at the same time, erasing the prior analog to
digital conversion previously held in the combined set-reset
latches and switch drivers in readiness for the next

conversion of a new analog value in the analog input sample-and-hold circuit (Figure 4).

To start the conversion process, the state machine will provide a BITSET(N) pulse, driving the output of NOR gate

5   NOR2 low, the output of inverter I3 high and the output of inverter I4 low. Since at this time the bit set signal BITSET(N-1) is low, the output of AND gate AND1 is low, as is the GLOBAL_RESET signal, so that the output of NOR gate NOR1 will be high, the output of inverter I1 low and the output of

10   inverter I2 high, thus changing the states of the four switch signals for the most significant bit of the digital-to-analog converter (see Figure 4). If the most significant bit is zero, the comparator (see Figure 4) will change state. This provides the REJECT signal shown in Figure 5. Now when the

15   bit select signal BITSELECT(N) goes low and BITSELECT(N-1) goes high, both inputs to AND gate AND1 will be high, thereby providing a high input to NOR gate NOR1. This is equivalent to a global reset signal for the switch drivers for that bit only, resetting the switch drivers for that bit. At the same

20   time, the BITSELECT(N-1) pulse initiates the setting of the switch drivers for the next bit to initiate the same sequence for bit N-1. If, on the other hand, the most significant (N) bit is a 1, the REJECT signal from the comparator will not change state. Consequently, the output of AND gate AND1 will

25   remain low and the switch drivers for the most significant

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bit will not be reset. Consequently the most significant bit has been determined and effectively stored in the combined set-reset latch and switch drivers, with the process being successively repeated for the remaining bits.

5   From the description above, it may be seen that in this embodiment, the testing of the state of the REJECT signal for any one bit is initiated by the same BITSET signal that initiates the setting of the combined set-reset latch and switch drivers for the next bit. For bit 0, there is no

10   "next" bit. Accordingly, the state machine may be programmed to provide a REJ_EN(0) signal equivalent to a further BITSET signal to test the state of the REJECT signal for the 0 bit to reset or not reset the combined set-reset latch and switch drivers as appropriate for the final step in an analog to

15   digital successive approximation conversion. Now, as another analog sample is taken, the digital value may be clocked out of the combined set-reset latches and switch drivers and the combined set-reset latches and switch drivers reset to start another analog to digital conversion.

20   Figures 6a through 6f are examples of some combined set-reset latches and switch drivers that may be used in the present invention. Figure 6a is a NOR gate based set-reset latch, Figure 6b shows a NAND gate based set-reset latch, and Figure 6c shows a NAND gate based set-reset latch with

reset enable and set enable. Figure 6d shows a NOR gate based set-reset latch with reset enable and global reset controls like that used in the example of Figure 5, and Figure 6e shows a NOR gate based set-reset latch with reset

5   enable and global reset controls using a hybrid gate, specifically a compound AOI gate. (An AOI gate logically is an AND-OR-Invert gate, though typically is realized by a circuit not having the intermediate AND signal suggested by its name.) Finally Figure 6f shows a NOR gate based set-

10 reset latch with reset enable and global set and reset controls using a compound AOI gate. Any of these set-reset latches may be easily adapted for use in an embodiment of the invention like that of Figure 4 by one of ordinary skill in the art.

15   Now referring to Figure 7, a NOR gate based combined set-reset latch and switch drivers duplicating the function of the NOR gate based combined set-reset latches and switch drivers of Figure 5, but further incorporating a level shift capability may be seen. The GLOBAL_RESET, BITSET and REJECT

20 signals may all be referenced to a first supply voltage, and the transistor level NOR gates referenced to a second, typically higher voltage power supply. Thus the switch driver signals may be higher voltage signals if desired.

In the circuit of Figure 7, the inverters I1 through I4 are connected and function the same as the inverters I1 through I4 of Figure 5. Considering the circuit comprising transistors Q1 through Q4, if either BITSET(n) or OUTP or

5 both are high, transistor Q1 or transistor Q2 or both will be on and transistor Q3 or transistor Q4 or both will be off. Therefore if any input is high, the output will be low. If all inputs are low, the output will be high, all in accordance with NOR gate logic states. The operation of the

10 circuit comprising transistors Q5 through Q10 is similar, differing only in that it has three inputs, all of which must be low to turn off all of transistors Q5, Q6 and Q7 and to turn on all of transistors Q8, Q9 and Q10 to provide a high state output. Finally, AND gate AND1 performs the same

15 function as AND gate AND1 of Figure 5. Of course for n = 0, the signal BITSET(n-1) becomes the signal REL_EN(0) of Figure 5.

In the embodiment of Figure 7, transistors Q3, Q8 and Q9 will not be completely turned off by a high on the low-

20 voltage inputs. The feedback connections serve to completely turn off Q4 and Q10 and cut off the supply current path, completing the level-shift. Also, while this example is for NOR gate based combined set-reset latch and switch drivers with level shifting, other circuits such as those of Figures

25 6b through 6f may be adapted for such combined use.

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Thus it may be seen that the present invention provides set-reset latches in successive approximation ADCs that themselves provide the non-overlapping switch driver outputs as latch outputs, rather than having each latch drive a

5   separate non-overlapping switch driver circuit. The present invention further provides the option of adding level shifting to the non-overlapping switch driver outputs of the set-reset latches, if desired. The latches themselves may be used in circuits other than ADCs. By way of example, Figure

10   8 shows a more generalized prior art level shifter and non-overlapping switch driver similar to that of Figure 3, with Figure 9 showing a present invention equivalent circuit similar to that of Figure 7. Figure 10 shows a prior art latch and non-overlapping switch driver, NOR gates NOR1 and

15   NOR2 being coupled as a set-reset latch, with Figure 11 showing a present invention equivalent. Figure 12 shows a prior art latch, level shifter and non-overlapping switch driver, with Figure 13 showing the present invention equivalent. In that regard, Figure 13 is similar to Figure

20   11, though with the circuit being powered from a different voltage than the logic supplying the input controls, typically a higher voltage.

While certain preferred embodiments of the present invention have been disclosed and described herein, it will

25   be understood by those skilled in the art that various

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changes in form and detail may be made therein without departing from the spirit and scope of the invention.